FPGA based 10G Performance Tester for HW OpenFlow Switch

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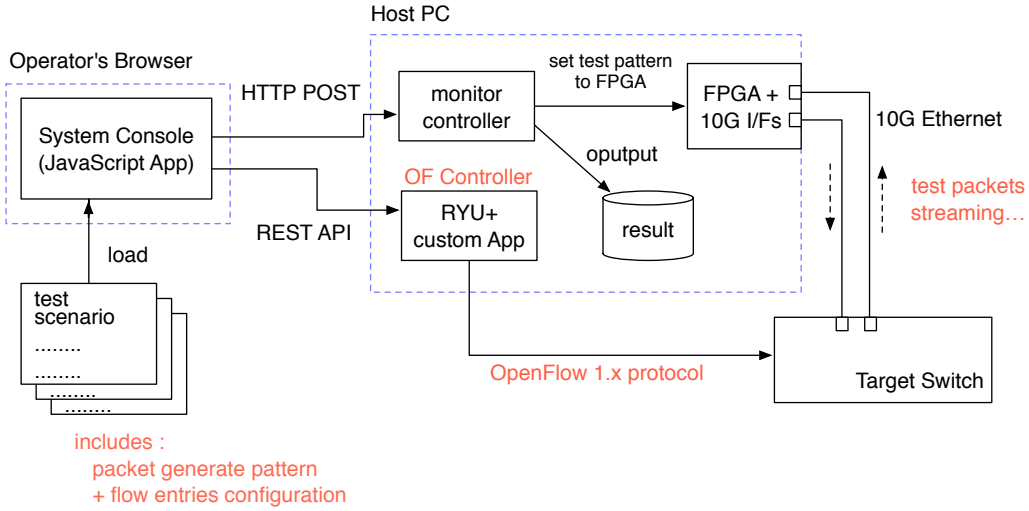
SDN operators need to measure the performance of OF HW switch on their site. Cause there is 1000 times differences in latency, depends on the specified flow entry. ASIC can forward in several µsecs but the software (CPU) may takes msec.

But it is not always documented. Features reply is not enough to describe it. And the high precision monitor such as IXIA and Spirent is too expensive for the site-admin.

Since my project, the FPGA based performance tester is designed to satisfy both of the accuracy (8ns) and the cost, in 10G range.

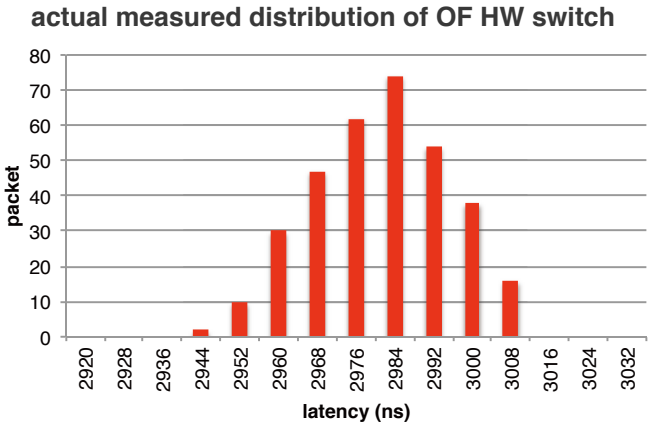
System Overview :



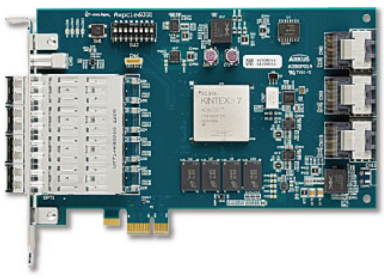
Output :

Not only the pps and bps, but also the latency distribution as a histogram are available.
(see the right figure →)

Internally, latency is counted as 4 levels of granularity. each counter has 1024 bins. (count in 8ns width (<184ns), 128ns (<131usec), 2048ns (<2ms), 131us (<134sec))



Component :



Xilinx Kintex-7, 125MHz
10G (SFP+) x4
Hardware TCP/UDP implement
PCIe gen2 x1 (just for control)

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